AMENDMENTS TO THE DRAWINGS

Applicants have amended FIGS. 1C and 1D, which are included on the Replacement Sheet attached to this Amendment. Applicants have amended FIG. 1C by adding a label for the surface portion, now labeled 162, and amended FIG. 1D by adding a label for the unreacted portion, now labeled 164. Both the surface portion and the unreacted portion are described at paragraph [0019]. No new matter is added by these amendments.

REMARKS

Claims 1–8, 10, 11, 13–21, and 26–28 are pending in this application and stand rejected. Claim 21 is withdrawn from consideration. Applicants have amended claims 1, 20, and 26 to address Examiner's objection to claim 1 regarding the unreacted portion of the SiGe surface layer. Applicants submit that one of ordinary skill in the art would understand what is meant by the unreacted portion and how that portion remains unreacted after reading the written description. However, Applicants have amended claims 1, 20, and 26 to recite that the SiGe surface layer has a base portion and that the base portion remains unreacted by oxidizing. No new matter is added by these claim amendments, nor do the amendments require further search, such that entry after-final is requested.

Applicants have amended FIGS. 1C and 1D to add labels for the surface portion 162 and the unreacted portion 164 or base portion of the SiGe surface layer, respectively. Applicants have consequently amended paragraph [0019] by adding labels 162 and 164 to the surface portion and unreacted portion or base portion of the SiGe surface layer, respectively, as described in that paragraph. No new matter is added by Applicants' amendments to the figures or specification. Applicants respectfully request reconsideration in view of the following remarks.

I. Rejections under 35 U.S.C. §103(a)

Claims 1–3, 13–16, 18–20, and 26–28 stand rejected under § 103(a) as being unpatentable over U.S. Patent No. 6,632,729 to Paton ("Paton") in view of Effects of low-temperature water vapor annealing of strained SiGe surface-channel pMOSFETs with high-k dielectric to Westlinder et al. ("Westlinder") and U.S. Patent No. 6,909,151 to Hareland et al. ("Hareland"). Amended claims 1, 20, and 26 are independent claims. Claims 2, 3, 13–16, 18, and 19 depend directly or indirectly from amended claim 1, and claims 27 and 28 depend directly from amended claim 26. Applicants respectfully traverse the rejections.

In the rejection, Examiner correctly notes that Paton fails to disclose forming a SiGe surface layer having an average Ge content of less than about 10 at.% on a

substrate and that Paton fails to disclose a SiGe surface layer where the oxidizing of the surface portion of the SiGe surface layer substantially prevents oxidation of the Si substrate during the depositing of the high-k dielectric or annealing process. (See the Office Action, page 4, ¶3 and pages 4–5, ¶4.) Examiner cites Westlinder as describing a SiGe layer on a substrate and as describing that oxidizing the surface portion of the SiGe surface layer substantially prevents oxidation of the Si substrate during depositing of the high-k dielectric or during an annealing process. Id. Examiner reasons that one of ordinary skill in the art would modify Paton in view of Hareland to include a SiGe surface layer as taught by Westlinder in order to improve device properties such as channel mobility and stability. Id.

Applicants submit that the Examiner has overlooked what the cited references describe and has presumed that the cited references disclose or suggest what they do not. In addition, Applicants submit that Examiner's stated reason for making the combination of references does not logically follow from the references themselves. Examiner does not provide any additional reasoning. Thus, the Examiner's case is not factually or rationally supported as is required. Obviousness is a question of law based on underlying factual inquiries. The factual inquiries were enunciated by the Court in *Graham v. John Deere Co.*, 148 USPQ 459 (1966). Additionally, the key to supporting any rejection under 35 U.S.C. §103 is the clear articulation of the reason(s) why the claimed invention would have been obvious in view of all of the factual information. See *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007).

Applicants submit that Examiner's rationale is not supported by the description given in Paton, as Examiner alleges, and is, in fact, contrary to that description. Specifically, Paton describes that a low-k silicon oxide layer formed on Si-containing substrates disadvantageously increases the Effective Oxide Thickness (EOT). That is, the low-k silicon oxide layer mitigates the benefit of the use of a high-k dielectric layer. (See Paton, col. 2, ll. 47–49.) At a minimum then, Paton provides that the device properties, like EOT, are not improved when a low-k silicon oxide layer is formed on a Si or Si-containing substrate. Paton makes this clear. Furthermore, Paton describes that this disadvantageous low-k silicon oxide layer is associated with "Si-containing" substrates.

(See Paton, col. 2, ll. 40–41.) It follows that the substrate compositions listed at column 3, lines 51–57, in Paton are the substrate compositions that Paton considers as exhibiting the disadvantageous low-k silicon oxide layer formation. Applicants note that Paton implicates the entire range of Ge in silicon substrates as exhibiting this problem. Based on Paton then, one of ordinary skill in the art would come to the conclusion that a SiGe layer on a substrate would have the same problem that Paton describes, and, for this reason alone, would not make the combination as the Examiner has done. Paton fails to recognize any device property improvement associated with utilizing substrates containing silicon with an average germanium content less than about 10 at.%. Stated another way, Applicants submit that one of ordinary skill in the art, having reviewed Paton, would not have a reasonable expectation of successfully making the proposed combination to improve device properties as alleged. None of the references cited cure this deficiency. For at least these reasons, Examiner's rationale does not support the alleged combination and Examiner has failed to establish a *prima facie* case of obviousness. Applicants respectfully request withdrawal of the rejection.

In addition, Applicants submit the Westlinder fails to factually support Examiner's case. Amended claim 1 recites, in part:

> forming an oxide layer between the high-k dielectric layer and the base portion of the SiGe surface layer by oxidizing the surface portion of the SiGe surface layer, the oxide layer being formed during one or both of said depositing and an annealing process after said depositing, wherein oxidizing the surface portion of the SiGe surface layer substantially prevents oxidation of the Si substrate during the depositing of the high-k dielectric layer or the annealing process, and wherein the base portion remains unreacted by the oxidizing. (Emphasis added.)

While Applicants note that Examiner references Westlinder for the proposition that oxidizing the surface portion of the SiGe surface layer substantially prevents oxidation of the Si substrate, this is not what Westlinder describes or suggests. Applicants note that Westlinder's "native" oxide layer is clearly formed before depositing the high-k layer, not between the layers during one or both of the depositing and an annealing process after

depositing the high-k dielectric layer as is recited in the claims. In other words, Westlinder's oxide layer is formed at the wrong time. Westlinder's oxide layer is formed prior to depositing a high-k dielectric layer–it is not formed between the high-k and SiGe layers. Since Westlinder's oxide layer is formed at the wrong time, it follows that what Westlinder additionally describes with respect to the oxide layer is irrelevant to Applicants' claimed invention.

For instance, Applicants submit that one of ordinary skill would not equate the effects of an oxide layer formed by wet chemical oxidation prior to depositing the high-k dielectric layer with an oxide layer formed between a high-k layer and an unreacted base portion of a SiGe surface layer as recited in amended claim 1. One of ordinary skill in the art would note that the results in going from one to the other are unpredictable. Therefore, Examiner cannot rely on Westlinder for describing that oxidizing the surface portion of the SiGe surface layer substantially prevents oxidation of the Si substrate, as claimed.

For similar reasons, Applicants submit that Westlinder fails to suggest that an oxide layer formed during one or both of depositing of a high-k layer and annealing after depositing would substantially prevent oxidation of the Si substrate during depositing of a high-k dielectric layer or during annealing after said depositing. Simply put, it is not logical to suggest that Westlinder's oxide layer, which is formed via a wet chemical process at the wrong time, would necessarily affect the substrate in the same way as an oxide layer formed according to the claimed invention. For the reasons set forth above, Westlinder does not factually support Examiner's case. For at least these additional reasons, Examiner has failed to establish a *prima facie* case of obviousness. Applicants respectfully request withdrawal of the rejections.

Furthermore, Examiner suggests that the oxide layer of Westlinder prevents oxidation of the substrate during depositing of the high-k dielectric layer or during annealing because Westlinder does not describe oxide formation between the SiGe layer and the substrate. (See parenthetical on page 4, ¶4.) Applicants submit that this is not supported by Westlinder either. Examiner suggests that Fig. 1 of Westlinder supports this interpretation. Applicants submit, however, that Fig. 1 depicts a schematic picture of the

stack and thus does not represent reality. (See Westlinder, page 525, 2nd sentence of "2. Experimental" paragraph) After all, Westlinder describes an oxide layer formed by a wet chemical process on the SiGe layer, but this oxide layer is not shown in the figure. Furthermore, in addition to the wrong timing of the oxide layer formation, set forth above, Westlinder does not describe the interface between the SiGe layer and the Si substrate at all. Westlinder is silent in this regard. Indeed, Westlinder is a journal article where the focus "is set on studying the interface between the high-k dielectric and the SiGe surface channel by performing water vapor annealing at 300°C." (See page 525, top of right column.) The interface between the SiGe layer and the Si buffer was not the focus of the study. Westlinder is silent regarding this interface, and silence cannot teach nor can it suggest anything to one of ordinary skill in the art. In sum, Westlinder fails to factually support any of Examiner's assertions; Applicants respectfully request withdrawal of the rejections.

Examiner references Hareland for the proposition that one of ordinary skill in the art would modify Paton in view of Westlinder and deposit a SiGe surface layer having an average Ge content less than about 10 at.% on a Si substrate. However, while Examiner references Westlinder for teaching a SiGe surface layer, Examiner fails to reconcile why one of ordinary skill in the art would ignore the higher Ge content described in Westlinder (i.e., $Ge_{0.2}Si_{0.8}$ or 20 at.% Ge and $Ge_{0.3}Si_{0.7}$ or 30 at.% Ge) in favor of the Ge content of Hareland. Applicants submit that no objective reason exists and this amounts to picking and choosing among the references using Applicants claims as a guide. For at least this reason, Examiner has failed to establish a *prima facie* case of obviousness. Applicants request withdrawal of the rejection.

Because claims 2, 3, 13–16, 18, and 19 depend directly or indirectly from amended claim 1, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, each of these claims recites a unique combination of elements not disclosed or suggested by Paton in view of Hareland and Westlinder.

Additionally, with respect to amended claim 20, Examiner notes that Paton fails to explicitly disclose the oxide layer formed by exposing the substrate to an oxygen

containing gas. (See Office Action, page 8, ¶1.) Examiner reference Westlinder as disclosing this subject matter. In particular, Examiner states that Westlinder discloses an oxide layer formed by exposing the substrate to a water vapor anneal. Id. However, amended claim 20 recites in pertinent part:

> wherein at least one of the depositing and the annealing comprises oxidizing the surface portion of the SiGe surface layer by exposing the SiGe surface layer to an oxygen-containing gas to form an oxide layer between the high-k dielectric layer and the base portion of the SiGe surface layer, wherein oxidizing the surface portion of the SiGe surface layer substantially prevents oxidation of the Si substrate during the depositing or the annealing, and wherein the base portion remains unreacted by the oxidizing. (Emphasis added.)

As set forth above, in Westlinder, the oxide layer is formed prior to depositing the high-k dielectric layer. Westlinder specifically suggests that the thin native oxide forms prior to ALCVD processing specifically when the wafers were cleaned in diluted HF and rinsed in de-ionized water. (See Westlinder, page 525, 1st full paragraph.) The oxide layer is formed via wet chemical oxidation, not by exposing the wafer to an oxygen-containing gas. So, Westlinder does not expressly suggest an oxide layer formed according to amended claim 20.

Regarding water vapor annealing process relied on by Examiner, Westlinder states that, in conjunction with the discussion of Fig. 7 on page 527 and with regard to the $Al_2O_3/Si_{0.8}Ge_{0.2}$ stack, "no reaction has taken place among the materials in the gate stack." Applicants submit that oxidation is by definition a reaction. Thus, even though Westlinder's oxide layer is already present prior to water vapor annealing, Westlinder explicitly states that no reaction (of any layer) occurs due to exposure to water vapor. In other words, based on Westlinder, one of ordinary skill in the art would not expect that water vapor annealing at the times and temperatures provided would form an oxide layer, as claimed.

As with the rejections of amended claims 1 and 20 above, Examiner rejects claim 26 over a combination of Paton in view of Hareland and Westlinder. For at least the

same reasons set forth above, Applicants submit that the references fail to teach or suggest the claimed invention and that one of ordinary skill in the art would not reasonably expect to successfully improve device properties as Examiner alleges. Thus, Applicants submit that Examiner has failed to establish a *prima facie* case of obviousness with respect to amended claim 26 and respectfully request withdrawal of the rejections. Because claims 27 and 28 depend directly or indirectly from amended claim 26, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, each of these claims recites a unique combination of elements not disclosed or suggested by Paton in view of Hareland and Westlinder.

Examiner rejects claims 4–8 under 35 U.S.C. §103(a) as being unpatentable over Paton in view of Westlinder, Hareland, and EP 0684 650 B1 to Hiroshi et al. ("Hiroshi"). Claims 4–8 depend directly or indirectly from amended claim 1. Applicants respectfully traverse the rejections. Examiner references Hiroshi as disclosing forming the SiGe surface layer by exposing the substrate to a process gas including a Ge-containing gas comprising at least one of GeH_4 or $GeCl_4$, according to claims 4 and 5. Examiner also reference Hiroshi as disclosing a process gas that comprises a Si-containing gas where the Si-containing gas comprises at least one of SiH_4, Si_2H_6, or SiH_2Cl_2, according to claims 7 and 8. The arguments presented above for amended claim 1 apply equally to this rejection. Applicants submit that Hiroshi fails to cure the deficiencies of Paton in view of Westlinder and Hareland described above. Applicants respectfully request withdrawal of the rejections.

Examiner rejects claims 10 and 11 under 35 U.S.C. §103(a) as being unpatentable over Paton in view of Westlinder, Hareland, and U.S. Pub. No. 2003/0218189 to Christiansen et al. ("Christiansen"). Claims 10 and 11 depend from amended claim 1. Applicants respectfully traverse the rejections.

Examiner references Paton in view of Hareland as disclosing the method recited in amended claim 1. Examiner admits that Paton fails to disclose the SiGe surface layer comprising a plurality of SiGe sublayers each with different Ge content, as recited in claim 10. Examiner references Christiansen as disclosing this subject matter, stating that it would have been obvious to one of ordinary skill in the art at the time of the invention to

modify Paton accordingly to reduce defects normally present in a single SiGe layer. (See Office Action, bottom of page 12 to page 13.)

The arguments presented above for amended claim 1 apply equally to this rejection. As set forth above, the combination of Paton in view of Hareland and Westlinder does not teach or suggest the invention claimed in amended claim 1. Christiansen fails to cure the deficiencies of Paton in view of Hareland and Westlinder. Examiner has failed to establish a *prima facie* case of obviousness with respect to claims 10 or 11. Applicants respectfully request withdrawal of the rejections.

Examiner rejects claim 17 under 35 U.S.C. §103(a) as being unpatentable over Paton in view of Westlinder, Hareland, and U.S. Patent No. 5,259,881 to Edwards et al. ("Edwards"). Claim 17 depends from amended claim 1. Applicants respectfully traverse the rejection.

Examiner references Paton in view of Hareland according to the rejection of amended claim 1 for rejecting claim 17 and references Edwards as teaching introducing a substrate into a process chamber of a batch-type processing system. The arguments presented above for amended claim 1 apply equally to this rejection. As set forth above, the combination of Paton in view of Hareland and Westlinder does not teach or suggest the invention claimed in amended claim 1. Applicants submit that Edwards fails to cure the deficiencies of Paton in view of Hareland and Westlinder referenced above. Therefore, Examiner has failed to establish a *prima facie* case of obviousness with respect to claim 17. Applicants respectfully request withdrawal of the rejection.

II. Conclusion

In view of the foregoing remarks and amendments, Applicants respectfully believe this case is in condition for allowance and respectfully request entry of the claim amendments and allowance of the pending claims. If the Examiner believes any detailed language of the claims requires further discussion, the Examiner is respectfully asked to telephone the undersigned attorney so that the matter may be promptly resolved. The Examiner's prompt attention to this matter is appreciated.

Applicants believe the response to be timely filed within two-months of the mailing date of the Office Action. Applicants are of the opinion that no fee is due as a result of this Response. If any charges or credits are necessary to complete this communication, please apply them to Deposit Account No. 23-3000.

Respectfully submitted,

WOOD, HERRON & EVANS L.L.P.

By: /Kevin E. Kuehn/
Kevin E. Kuehn, Reg. No. 51,904

2700 Carew Tower
441 Vine Street
Cincinnati, OH 45202
513/241-2324 (voice)
513/241-6234 (facsimile)

991053v1